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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,916	01/29/2004	Toshio Miyamoto	843.41648VX1	2643

20457 7590 12/10/2004

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EXAMINER	
GARCIA, JOANNIE A	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,916	MIYAMOTO ET AL.	
	Examiner	Art Unit	
	Joannie A Garcia	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 6,7 and 10 is/are rejected.

7)☒ Claim(s) 1-5,8,9,11 and 12 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 02-03-04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 1-12 are objected to because of the following informalities:

In claims 1 and 6, line 12, "layers" after "passivation", should be replaced with --layer--.

In claims 1 and 6, line 16, "layers" after "passivation", should be replaced with --layer--.

The term "predetermined" in claims 1, 5, and 6, is a relative term, which renders the claims indefinite. The term "predetermined" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. If applicant intends a particular fuse opening, and particular characteristics of the plurality of memory cells, it should be clearly recited.

Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 6 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawakita et al (U.S. Patent 6,372,554).

Kawakita et al discloses manufacturing a semiconductor integrated circuit device comprising, forming a plurality of memory cells in a plurality of chip areas on a main surface of a semiconductor wafer (Figure 15), forming a plurality of multi-layered first wirings 58 in an upper layer of said plurality of memory cells (Figures 15 and 19), forming a plurality of fuses

Fa/Fb in said plurality of chip areas (Figures 15 and 19), forming a passivation layer 51/60 over said plurality of first wirings and said plurality of fuses (Figures 15 and 19), and removing parts of said passivation layer to expose a wiring in the same layer as the upper most wiring of said plurality of first wirings, thereby forming a plurality of internal connection terminals 66 (Figures 15 and 19), removing other parts of said passivation layer, thereby forming fuse openings 55 over each of said plurality of fuses (Figure 15 and 19), after forming said passivation layer, conducting a probe test to detect presence of defect cells, and irradiating laser to said fuse through a fuse opening of said plurality of fuse openings, thereby cutting said fuse by fusion when said probe test detects defect cells (Column 1, lines 53-58), forming a plurality of second wirings 70 having one ends electrically connected to said internal connection terminals over said passivation layer (Figures 15 and 19), wherein at least a part of said plurality of second wirings are arranged over at least a part of said plurality of fuses (Figure 15), then forming an uppermost protection layer 72 on said plurality of second wirings and removing a part of said uppermost protection layer (Figures 15 and 19), thereby selectively exposing the other ends of said plurality of second wirings (Figure 19), performing a heat treatment to said uppermost protection layer, thereby curing said uppermost protection layer (Column 2, lines 10-27, and Column 9), forming a plurality of external connection terminals TP at the other ends of said plurality of second wirings (Figure 19), then cutting said semiconductor wafer into said chip areas, thereby obtaining a plurality of semiconductor chips (Column 10, lines 17-23).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakita et al as applied to claims 6 and 10 above, and further in view of the following comments.

With respect to claim 7, Kawakita et al discloses the claimed invention except for heating at a temperature of 260 °C. It would have been obvious to one having ordinary skill in the art at the time the invention was made to determine a suitable temperature, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

In addition, the selection of a suitable temperature, is obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species of result effective variables. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996)(claimed ranges or a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill or art) and In re Aller, 105 USPQ 233 (CCPA 1995) (selection of optimum ranges within prior art general conditions is obvious).

Note that the specification contains no disclosure of either the critical nature of the claimed temperatures or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen temperatures or upon another variable recited in a claim, the Applicant must show that the chosen temperatures are critical. *In re Woodruf,* 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claims 8, 9, 11, and 12, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-5 would be allowable if rewritten to overcome the objection(s) set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 1 would be allowable if rewritten or amended to overcome the objection(s) set forth in this Office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joannie García whose telephone number is (571) 272-1861. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Fourson
Primary Examiner
Art Unit 2823

JAG
November 29, 2004

GFourson
Primary Examiner